(19) Japan Patent Office (JP)
(12) KOKAI TOKKYO KOHO (A)
(11) Laid-open Application Number: Heisei 6-53075
(43) Publication Date: February 25, 1994

(51) Int. Cl.[5]	Id. Symbol		Office Ref. No.	F1	Techn. Ind. Field
H 01 G 4/12	346				
H 01 G 4/30	301	A	8019-5E		
		D	8019-5E		
H 01 G 4/42	331		9174-5E		

Examination Request: None No. of Claims: 1 (total pages 6)

(21) Application No.: Heisei 4-219719
(22) Application Filed: July 27, 1992

(71) Applicant: 000006264
Mitsubishi Materials Co., Ltd.
Address: 1-5-1, Ote-machi, Chiyoda-ku, Tokyo
(72) Inventor: Daanaru Pii Baakusu
Address: 2270, Daigaku Yokose, Yokose-machi, Akichichi, Saitama-ken
c/o Mitsubishi Materials Co., Ltd., Ceramics Laboratory

(54) [Title of the Invention] MULTILAYER CERAMIC CAPACITOR FOR BALANCED LINE

(57) [Abstract]

[Object] It is an object of the present invention to provide a small-size multilayer ceramic capacitor which can be mounted with a high density on a circuit substrate with a small mounting area, thereby making it possible to decrease the size of electronic devices, and which can improve the filter response and remove a high-frequency noise.

[Structure] A laminate 45 is formed by alternately laminating a dielectric sheet 10 having formed on its surface an inner electrode 10a which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side, a dielectric sheet 20 having formed on its surface an inner electrode 20a which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side, and a dielectric sheet 30 having formed on its surface an inner electrode 30a which is extended to the two mutually opposite outer sides, to which electrodes 10a, 20a are not extended, and is located at a certain distance from the two mutually opposite outer sides, to which electrodes 10a, 20a are extended. A pair of outer electrodes 41, 42 which are connected to electrodes 10a, 20a are formed on both side surfaces of the laminate, and outer electrodes 43 connected to electrode 30a are

formed on other two side surfaces of the laminate. Three capacitors are incorporated, and three terminals are integrated.

[Patent Claims]

[Claim 1] A multilayer ceramic capacitor for a balanced line comprising

a laminate (45) formed by alternately laminating

a first rectangular ceramic dielectric sheet (10) having formed on its surface a first inner electrode (10a) which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side,

a second rectangular ceramic dielectric sheet (20) having formed on its surface a second inner electrode (20a) which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side,

and a third ceramic dielectric sheet (30) having formed on its surface a third inner electrode (30a) which is extended to the two mutually opposite outer sides to which said first and second electrodes (10a, 20a) are not extended and is located at a certain distance from the two mutually opposite outer sides to which said electrodes (10a, 20a) are extended,

a pair of a first and second outer electrodes (41, 42) for connecting a balanced line, which are formed on both side surfaces of said laminate (45) and are connected to said first and second inner electrodes (10a, 20a), and

third outer electrodes (43) for grounding, which are formed on other two side surfaces of said laminate (45) and are connected to said third inner electrode (30a).

[0001]

[Detailed Description of the Invention]

[Field of Industrial Utilization] The present invention relates to a multilayer ceramic capacitor suitable as a chip noise filter for balanced lines of communication circuits such as telephones and modems, or power supply circuits such as DC-DC converters. More specifically, the present invention relates to a chip bypass capacitor suitable for absorbing electromagnetic interference, in which three capacitors are incorporated and three terminals are integrated.

[0002]

[Prior Art Technology] Three wire balanced lines consisting of a pair of input lines and a ground line are suitable for the communication circuits of power supply circuits of the above-described type. Low-pass filters or bypass filters are required to remove a common-mode noise and differential noise in such lines. More specifically, a filter is often used in which, as shown in Fig 17, a multilayer ceramic capacitor C_1 is connected between the input line A and ground line G, a multilayer ceramic capacitor C_2 is connected between the input line B and ground line G, and a multilayer ceramic capacitor C_3 is connected between input lines A and B. Each of the above-mentioned three multilayer ceramic capacitors comprises a laminate and a pair of external electrodes. The

laminate is obtained by preparing two of rectangular ceramic dielectric sheets each having formed on its surface an inner electrode which is extended to one outer side of the sheet and is located at a certain distance from the sheet outer side which is opposite to the above-mentioned sheet outer side, stacking those two ceramic dielectric sheets so that the sheet outer sides with the inner electrodes extended thereto are on respective opposite sides, and laminating and integrating a plurality of such stacked and assembled ceramic dielectric sheets. A pair of outer electrodes is formed so as to be connected to the respective inner electrodes exposed on both side surfaces of the laminate. Those three capacitors are separately mounted on a printed circuit board.

[0003]

[Problems Addressed by the Invention] Thus, in the conventional filters consisting of the above-described three multilayer ceramic capacitors, the capacitors were separately mounted on a substrate. As a result the printed circuit was complex and the noise absorption capability of the filter was degraded due to the residual impedance of the printed circuit. Furthermore, when the capacitor was mounted on a substrate, the substrate was required to have a large mounting area, and the size of electronic devices was difficult to decrease. It is an object of the present invention to provide a small-size, multilayer ceramic capacitor for a balanced line, which can be mounted with a high density on a circuit substrate with a small mounting area, thereby making it possible to decrease the size of electronic devices. Another object of the present invention is to provide a multilayer ceramic capacitor for a balanced line, which makes it possible to improve filter response and to remove a common-mode noise and differential noise in a three-wire balanced line by incorporating three capacitors close to each other in a single element and integrating three terminals.

[0004]

[Means to Resolve the Problems] The structure of the present invention designed to attain the above-described object will be described below with reference to Fig 1, Fig 5, and Fig 8. In a multilayer ceramic capacitor 50 in accordance with the present invention, a laminate 45 is formed by alternately laminating a first rectangular ceramic dielectric sheet 10 having formed on its surface a first inner electrode 10a which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side, a second rectangular ceramic dielectric sheet 20 having formed on its surface a second inner electrode which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side, and a third ceramic dielectric sheet 30 having formed on its surface a third inner electrode 30a which reaches the two mutually opposite outer sides to which the two electrodes 10a, 20a were not extended and is located at a certain distance from the two mutually opposite outer sides to which the two electrode 10a, 20a were extended. Furthermore, a first and second outer electrodes 41, 42 for a balanced line connection, which are connected to the electrodes 10a, 20a, respectively, are formed on both side surfaces of laminate 45, and third outer electrodes 43 for grounding, which are connected to the third inner electrode 30a, are formed on other two side surfaces of laminate 45.

[0005]

[Operation] As shown in Fig 8, when capacitor 50 is connected to lines A, B, and G, a capacitor C_3 for absorbing a differential noise is formed between the first outer electrode 41 and second outer electrode 42, and two capacitors C_1 and C_2 for absorbing a common-mode noise are formed between the first outer electrode 41 and third outer electrode 43, and between the second outer electrode 42 and third outer electrode 43, respectively. In the chip-like multilayer ceramic capacitor having the above-described structure, the three capacitors are located inside and three terminal electrodes 41, 42, 43 are integrated with side surfaces of laminate 45. Therefore, (1) the filter response is improved, and (2) three capacitors, which are implemented in a single element, take a very small space and can be mounted on a circuit substrate by a process involving few operations.

[0006]

[Embodiments] The embodiments of the present invention will be described below in greater detail with reference to the drawings attached.

<Embodiment 1> First, a large number of dielectric green sheets were prepared. Those dielectric green sheets were formed by coating a barium titanate-based dielectric slurry having a JIS-R characteristic by a doctor blade method on the upper surface of a polyester base sheet, followed by drying. Of those green sheets, a certain group was taken as first green sheets, another group was taken as second green sheets, and still another group was taken as third green sheets. Then, a conductive paste containing Ag/Pd as the main components was screen printed according to respective patterns on the surfaces of the first, second, and third green sheets, followed by drying for 4 min at a temperature of 80°C. Thus, as shown in Fig 5, a first inner electrode 10a was formed by printing on the surface of first green sheets 10 in such a manner that it was extended to one outer side and was located at a certain distance from the outer side opposite to the above-mentioned outer side. A second inner electrode 20a was formed by printing on the surface of second green ceramic green sheets in such a manner that it was extended to the above-mentioned opposite outer side and was located at a certain distance from the above-mentioned one outer side. Then, a cross-like third inner electrode 30a was formed by printing on the surface of third ceramic green sheets in such a manner that it was extended to two mutually opposite outer sides to which the two inner electrodes 10a, 20a were not extended and was located at a certain distance from the two mutually opposite outer sides to which the two inner electrodes 10a, 20a were extended. In this example, the three inner electrodes 10a, 20a, and 30a had the same surface area.

[0007] As shown in Fig 1 and Fig 5, in this example a first dielectric sheet 10, a third dielectric sheet 30, a second dielectric sheet 20, a first dielectric sheet 10, a third dielectric sheet 30, and a second dielectric sheet 20 were laminated on the second dielectric sheet 20 in the order of description. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 8 layers. This laminate 45 was integrated by

thermal pressing and fired for about 1 h at a temperature of 130°C to obtain a sintered body. The sintered body was barrel polished to expose the inner electrodes 10a, 20a, and 30a on the side surface of the sintered body (Fig 6). Both end portions of the sintered body where the inner electrodes 10a, 20a were exposed were coated with an electrically conductive paste containing Ag as the main component, and then the electrically conductive paste was coated on the whole periphery of the central portion of the sintered body where the inner electrode 30a was exposed. The electrically conductive paste in all of the above-mentioned regions was then fired to form the first and second outer electrodes 41, 42 and a third outer electrode 43. As a result, a multilayer ceramic capacitor 50 shown in Fig 7 was obtained.

[0008] In order to study characteristics of the multilayer ceramic capacitor 50, it was connected to a three-wire balanced line including a pair of input lines A and B and a ground line G (see Fig 8). More specifically, the first outer electrode 41 of the multilayer ceramic capacitor 50 was connected to line A, the second outer electrode 42 was connected to line B, and the third outer electrode 43 was connected to line G. When a signal to which a high-frequency noise, electromagnetic waves and the like were admixed was fed into the balanced line, a differential noise was absorbed between the first outer electrode 41 and second outer electrode 42, and the respective common-mode noise was absorbed between the first outer electrode 41 and third outer electrode 43, and between the second outer electrode 42 and third outer electrode 43. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$$C_1 = C_2 = C_3 \qquad (1)$$

[0009] <Embodiment 2> Figs 9 – 12 show a cross section of the multilayer ceramic capacitor of the second embodiment of the present invention. In those figures, structural components identical to those shown in Figs 1 – 4 are assigned with the same symbols. In this embodiment, the third dielectric sheet 30, second dielectric sheet 20, third dielectric sheet 30, first dielectric sheet 10, third dielectric sheet 30, and second dielectric sheet 20 were laminated in the order of description on the first dielectric sheet 10. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 8 layers. In this example, the surface area of inner electrode 30a was half of the surface area of each of the inner electrode 20a and inner electrode 30a. Other elements of the structure were identical to those of Embodiment 1, and their explanation is omitted to avoid redundancy. Characteristics of the multilayer ceramic capacitor were identical to those obtained in Embodiment 1. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$$C_1 = C_2 = C_3/2.5 \qquad (2)$$

[0010] <Embodiment 3> Figs 13 – 16 show a cross section of the multilayer ceramic capacitor of the third embodiment of the present invention. In those figures, structural components identical to those shown in Figs 1 – 4 are assigned with the same symbols. In

this embodiment, the first dielectric sheet 10, second dielectric sheet 20, third dielectric sheet 30, first dielectric sheet 10, second dielectric sheet 20, first dielectric sheet 10, third dielectric sheet 30, and second dielectric sheet 20 were laminated in the order of description on the second dielectric sheet 20. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 10 layers. In this example, the surface area of the three inner electrodes 10a, 20a, and 30a was the same. Other elements of the structure were identical to those of Embodiment 1, and their explanation is omitted to avoid redundancy. Characteristics of the multilayer ceramic capacitor were identical to those obtained in Embodiment 1. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$C_1 = C_2 = C_3/2$ (3)

[0011] Furthermore, the number of layers in the ceramic dielectric sheet in accordance with the present invention and the surface area of the third inner electrode 30a employed for grounding are not limited to the above-described embodiments and can be changed appropriately according to the required capacitance.

[0012]

[Effect of the Invention] As described above, the present invention provided a small capacitor in which three capacitors are incorporated in a single element and three terminals are integrated. As a result, mounting can be conducted by a process consisting of a small number of operations and a printed circuit substrate is not required to have a large mounting area. At the same time, the filter response can be improved. Furthermore, a common-mode noise and differential noise in three-wire balanced lines can be removed. Therefore, the capacitor in accordance with the present invention is suitable as a chip noise filter (CNF) absorbing electromagnetic interference (EMI). Another advantage of the capacitor in accordance with the present invention is that the capacitance of the incorporated capacitors can be changed by changing the surface area of the second inner electrode with respect to the surface area of the first inner electrode.

[Brief Description of the Drawings]

Fig 1 is a cross section along the line H-H in Fig 7 for which the relation $C_1 = C_2 = C_3$ is valid, this relation being obtained for the multilayer ceramic capacitor which is an embodiment of the present invention.

Fig 2 is a cross section along the line J-J relating to the same embodiment.

Fig 3 is a cross section along the line K-K relating to the same embodiment.

Fig 4 is a cross section along the line L-L relating to the same embodiment.

Fig 5 is a perspective view prior to lamination in a laminate preparation.

Fig 6 is a perspective view of a sintered body prepared by sintering the laminate.

Fig 7 is a perspective view of a multilayer ceramic capacitor fabricated by arranging first, second, and third outer electrodes on the sintered body.

Fig 8 is a circuit diagram illustrating connection of the multilayer ceramic capacitor to a balanced line.

Fig 9 is a cross section corresponding to Fig 1 for which the relation $C_1 = C_2 = C_3/2.5$ is valid, this relation being obtained for the multilayer ceramic capacitor which is another embodiment of the present invention.

Fig 10 is a cross section along the line M-M relating to the same embodiment.

Fig 11 is a cross section along the line N-N relating to the same embodiment.

Fig 13 is a cross section along the line O-O relating to the same embodiment.

Fig 9 is a cross section corresponding to Fig 1 for which the relation $C_1 = C_2 = C_3/2$ is valid, this relation being obtained for the multilayer ceramic capacitor which is another embodiment of the present invention.

Fig 14 is a cross section along the line P-P relating to the same embodiment.

Fig 15 is a cross section along the line Q-Q relating to the same embodiment.

Fig 16 is a cross section along the line R-R relating to the same embodiment.

Fig 17 is a circuit diagram illustrating connection of a conventional multilayer ceramic capacitor to a balanced line.

[Legends]

10 – first ceramic dielectric sheet (first ceramic green sheet)
10a – first inner electrode
20 – second ceramic dielectric sheet (second ceramic green sheet)
20a – second inner electrode
30 – third ceramic dielectric sheet (third ceramic green sheet)
30a – third inner electrode
41 – first outer electrode
42 – second outer electrode
43 – third outer electrode
45 – laminate
50 – multilayer ceramic capacitor

Fig 1

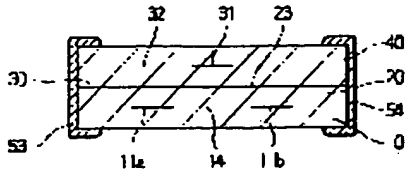
10 – first ceramic dielectric sheet (first ceramic green sheet)
10a – first inner electrode
20 – second ceramic dielectric sheet (second ceramic green sheet)
20a – second inner electrode
30 – third ceramic dielectric sheet (third ceramic green sheet)
30a – third inner electrode
41 – first outer electrode
42 – second outer electrode
43 – third outer electrode
50 – multilayer ceramic capacitor

Fig 2
Fig 3

Fig 4

Fig 5
45 – laminate

Fig 6
Fig 7
Fig 8
Fig 9
Fig 10
Fig 11
Fig 12
Fig 13
Fig 14
Fig 15
Fig 16
Fig 17



(57)Abstract:
PURPOSE: To prevent reliably the generation of crosstalk between signal lines even if internal conductors, which absorb a high-frequency noise and a surge and are connected to a plurality of the signal lines, are provided in a higher density.
CONSTITUTION: The title laminated capacitor array is a laminated material consisting of dielectric sheets 10, 20 and 30 having a capacitive property and varistor characteristics and the sheet 10 is provided with internal conductors 11a and 11b, which are connected to one side of the sheet 10 and are electrically insulated from the remaining three sides at an interval, on the sheet surface. The sheet 30 is provided with an internal conductor 31 on the sheet surface like the sheet 10. The sheet 20, which is used as an intermediate sheet, is provided with a ground conductor 23, which is insulated from one pair of sides, which respectively correspond to the one side, to which the conductors 11a and 11b are connected, of the sheet 10 and the one side, to which the conductor 31 is connected, of the sheet 30, and is connected to another one pair of sides, on the sheet surface and capacitances are respectively formed between the conductors 11a, 11b and 31 and the conductor 23 via the sheet 20 or 30. Electrodes for signal use, which are connected to the conductors 11a, 11b and 31, and one pair of electrodes 53 and 54 for grounding use, which are connected to the conductor 23, are formed on the side surfaces of the laminated material independently of each other.

11)Publication number : **06-053077**
(43)Date of publication of application : **25.02.1994**

(51)Int.CI. **H01G 4/40**
H01C 7/10

(21)Application number : **04-219720**
(22)Date of filing : **27.07.1992**

(71)Applicant : **MITSUBISHI MATERIALS CORP**
(72)Inventor : **SHIMURA MASARU**
WADA HIDEAKI

(54) **LAMINATED CAPACITOR ARRAY WITH VARISTOR FUNCTION**